WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a plurality of memory array areas respectively disposed along a first direction and a second direction, each memory array area including a plurality of bit lines extending in the first direction, a plurality of word lines extending in the second direction intersecting the first direction, and a plurality of memory cells provided in association with portions where said plurality of bit lines and said plurality of word lines intersect respectively;

a plurality of sense amplifier areas disposed alternately relative to said plurality of memory array areas disposed along the first direction;

a plurality of first common input/output lines associated with said plurality of memory array areas disposed along the first direction;

a second common input/output line connected to said plurality of first common input/output lines;

first selection circuits each provided between each of said plurality of first common input/output lines and said plurality of bit lines;

second selection circuits provided between said plurality of first common input/output lines and said second common input/output line;

a first select signal generating circuit which supplies a select signal to each of said plurality of first selection circuits; and

a second select signal generating circuit which produces a signal for selecting each of the word lines in said plurality of memory array areas disposed along the second direction,

wherein said second common input/output line has a signal transfer channel which extends in the second direction.

2. A semiconductor memory device according to claim 1, wherein said each memory cell is a dynamic memory cell which comprises a MOSFET and a capacitor and wherein the gate of MOSFET is defined as a selection terminal, one source or drain thereof is defined as an input/output terminal and the other source or drain thereof is connected to a storage node used as one electrode of said capacitor.

3. A semiconductor memory device according to claim 1, wherein said first common input/output lines comprise,

first wirings which extend over said sense amplifier areas in the second direction and are respectively connected to the bit lines in the corresponding memory array areas through the first selection circuits, and

second wirings which extend over said memory array areas in the second direction and extend outwardly of memory cell array areas comprised of said plurality of memory array areas so as to be connected to one ends of said second selection circuits respectively,

said at least one second common input/output line includes,

third signal lines which extend along the first direction outside said memory cell array areas as viewed in the second direction, and

said second selection circuits are respectively provided at portions where second signal lines and said third signal lines are respectively connected.

4. A semiconductor memory device according to claim 3, wherein said each second selection circuit comprises an amplifier circuit for amplifying a signal transferred between the first common input/output line and the second common input/output line according to a select signal.

5. A semiconductor memory device according to claim 3, wherein said memory cell array areas are provided at least two as viewed in the second direction of a semiconductor chip, and

the third signal lines of said second common input/output line are dispersedly disposed on both sides of said each memory cell array area as viewed in the second direction thereof.

6. A semiconductor memory device according to claim 5, wherein each of sub-word drivers for respectively selecting the word lines is provided between the memory array areas provided along the second direction, and said second select signal generating circuit for forming a signal for selecting one of the word lines, which corresponds to said each memory cell array area, is provided inside the semiconductor chip.

7. A semiconductor memory device according to claim 6, wherein said second common input/output line further includes fourth signal lines each of which is connected to said each third signal line extended in the first direction and is disposed so as to extend over said memory array area in the second direction and each of which connects a main amplifier for amplifying a signal read out from said each memory cell provided adjacent to said each second select signal generating circuit to a write amplifier for transferring a write signal to said memory cell.

8. A semiconductor memory device according to claim 7, wherein said fourth signal lines are disposed on a specific memory array area placed along the second

direction, and said main amplifier and write amplifier are provided in accordance with the layout of the fourth signal lines.

9. A semiconductor memory device according to claim 1, wherein the memory cell array areas comprising a plurality of memory array areas respectively disposed in the first and second directions are provided at least two in the second direction of the semiconductor chip,

each of sub-word driver areas for respectively selecting the word lines is provided between the memory array areas provided along the second direction, and

said second select signal generating circuit for forming a signal for selecting the word line is provided inside the semiconductor chip, and

said second common input/output line comprises,

fifth signal lines which extend along the sub-word driver areas and each of which is connected through said second selection circuit at a portion intersecting said each first common input/output line, and

sixth signal lines connected to said fifth signal lines and each of which extends over said each memory array area in the second direction and connects the main amplifier to write amplifier provided adjacent to said second select signal generating circuit.

10. A semiconductor memory device according to claim 8, wherein said memory cell array areas comprising a plurality of memory array areas respectively disposed in the first and second directions are provided two by two in the first and second directions of the semiconductor chip,

each of sub-word driver areas for respectively selecting the word lines is provided between the memory array areas provided along the second direction in each of said memory cell array areas,

said second select signal generating circuits corresponding to said memory cell array areas provided along the second direction are respectively provided inside the semiconductor chip, said

first select signal generating circuits corresponding to said memory cell array areas provided along the first direction are respectively provided inside the semiconductor chip,

the main amplifiers and write amplifiers provided in association with said four memory cell array areas are connected to a commonly provided input/output circuit through further provided third common input/output lines, and said

specific memory array area is placed in a specific position of said each memory cell array area as viewed in the first direction so that the third common input/output lines become shortest.

11. A semiconductor memory device according to claim 10, wherein said each memory cell array area has a first memory block and a second memory block divided into two in the first direction, said

first select signal generating circuit commonly supplies a select signal to said first memory block and

said second memory block, said second select signal generating circuit supplies a select signal to each of said first memory block and said second memory block, and

said specific memory array area is one located in the direction of the center of the chip, of the memory array areas provided for said first and second memory blocks as viewed in the first direction.

12. A semiconductor memory device according to claim 11, wherein each of said first common input/output lines and said second common input/output line comprises a pair for transferring complementary signals,

said amplifier circuit comprises a sub amplifier for reading and a buffer for writing,

said sub amplifier comprises differential type first and second MOSFETs having gates to which said first common input/output lines are connected, and having drains cross-connected to said second common input/output line, third and fourth MOSFETs which are respectively provided at the sources of said first and second MOSFETs and each of which forms an operating current according to a select signal, and a fifth MOSFET which is provided between the sources of the differential MOSFETs and turned off upon at least a write operation, and

said buffer comprises a CMOS buffer comprised of a pair of P channel type MOSFET and N channel type MOSFET for driving said first common input/output lines in response to complementary signals from said second common input/output line.

13. A semiconductor memory device according to claim 12, wherein said fifth MOSFET comprises two MOSFETs connected in parallel.

14. A semiconductor memory device comprising:

a plurality of memory array areas respectively disposed along a first direction and a second direction, each memory array area including a plurality of bit lines provided along the first direction, a plurality of word lines provided along the second direction orthogonal to the first direction, and a plurality of memory cells provided in association with portions where said plurality of bit lines and said plurality of word lines intersect respectively;

a plurality of sense amplifier areas disposed alternately relative to said plurality of memory array areas provided along the first direction;

a plurality of sub-word driver areas disposed alternately relative to said plurality of memory array areas provided along the second direction;

first common input/output lines provided in said sense amplifier areas and connected to their corresponding bit lines through first selection circuits; and

second common input/output lines respectively connected to said first common input/output lines through second selection circuits,

wherein said each second selection circuit comprises an amplifier circuit for amplifying a signal transferred between said first common input/output line and said second common input/output line according to a select signal,

said amplifier circuit comprises a sub amplifier for reading and a buffer for writing,

said sub amplifier comprises differential type first and second MOSFETs having gates to which said first common input/output lines are connected, and having drains cross-connected to said second common input/output lines, third and fourth MOSFETs which are respectively provided at the sources of said first and second MOSFETs and each of which forms an operating current according to a select signal, and a fifth

MOSFET which is provided between the sources of the differential MOSFET5 and turned off upon at least a write operation, and

said buffer comprises a CMOS buffer comprised of a pair of P channel type MOSFET and N channel type MOSFET for driving said first common input/output lines in response to complementary signals from said second common input/output lines.

15. A semiconductor memory device comprising:

a plurality of memory array areas disposed along a virtual line extending in a first direction;

a plurality of sense amplifier areas disposed alternately relative to said plurality of memory array areas;

a plurality of first common data lines which are provided in association with said plurality of sense amplifier areas and extend in a second direction intersecting said virtual line; and

a second common data line to which any of said plurality of first common data lines is selectively connected,

wherein said second common data line includes wirings which pass through any of said plurality of memory array areas and extend in the second direction.

16. A semiconductor memory device according to claim 15, wherein said plurality of memory array areas are respectively provided with a plurality of data lines which extend in the first direction, a plurality of word lines which extend in the second direction, and a plurality of dynamic memory cells provided in association with portion where said plurality of data lines and said plurality of word lines intersect respectively.

17. A semiconductor memory device comprising:

a plurality of first memory array areas disposed along a virtual line extending in a first direction;

a plurality of first sense amplifier areas disposed alternately relative to said plurality of first memory array areas;

a plurality of first sub common data lines which are provided in association with said plurality of first sense amplifier areas and extend in a second direction intersecting said virtual line;

a first main common data line extending in the first direction;

a plurality of first switch circuits respectively provided between said plurality of first sub common data lines and said first main common data line to selectively connect any of said plurality of first sub common data lines to said first main common data line;

a plurality of second memory array areas respectively disposed along said plurality of first memory array areas;

a plurality of second sense amplifier areas disposed alternately relative to said plurality of second memory array areas;

a plurality of second sub common data lines which are provided in association with said plurality of second sense amplifier areas and extend in the second direction;

a second main common data line extending in the first direction; and

a plurality of second switch circuits respectively provided between said plurality of second sub common data lines and said second main common data line to selectively connect any of said plurality of second sub common data lines to said second main common data line,

wherein said second main common data line is formed on the one side of portions divided into two with said plurality of first memory array areas as a boundary, and said plurality of second memory array areas are included on the other side.

18. A semiconductor memory device according to claim 17, wherein said plurality of first switch circuits and said plurality of second switch circuits are formed on said one side.